IN THE CLAIMS

1. (Currently amended) A method of fabricating a semiconductor substrate, comprising:

forming an isolation layer in a substrate of first conductivity type to define an active region;

diffusing impurities of second conductivity type in a predetermined region of the active region to form an impurity diffused region;

recessing a region of the isolation layer and exposing a portion of the substrate of first conductivity type ~~material~~ under the impurity-diffused region; and

forming a salicide layer ~~covering~~ on a surface of the impurity-diffused region and ~~covering~~ on a surface of the exposed portion of the substrate of first conductivity type.

2. (Previously presented) The method of claim 1, in which recessing a region of the isolation layer and exposing a portion of the substrate comprises etching the device isolation layer to a depth deeper than a depth of the impurity diffused region.

3. (Previously presented) The method of claim 1, in which the forming the salicide layer comprises:

forming metal on the impurity diffused region, on the active region, and on the walls of the recess; and

annealing the metal layer to diffuse atoms of the metal into portions of the active region in contact with the metal and into portions the substrate of first conductivity type in contact with the metal.

4. (Original) The method of claim 3, in which the metal comprises at least one material selected from the group consisting of cobalt, titanium, and nickel.

5. (Previously presented) A method of fabricating a semiconductor device, comprising:

forming a device isolation layer in a predetermined region of a substrate of first conductivity type to define an active region;

forming a gate pattern crossing the active region;

forming a source/drain region of second conductivity type in the active region at both sides of the gate pattern;

patterning the device isolation layer to form a recess in the device isolation layer that exposes a portion of the substrate of first conductivity type adjacent the source/drain region at one side of the gate pattern; and

siliciding a surface of the source/drain region of second conductivity type and a surface of the substrate of first conductivity type exposed by the recess.

6. (Previously presented) The method of claim 5, in which patterning the device isolation layer to form a recess comprises etching the device isolation layer to a depth deeper than the thickness of the source/drain region of second conductivity type.

7. (Previously presented) The method of claim 5, in which the forming the gate pattern comprises:

forming a gate insulation layer over the active region and a gate conductive layer over the gate insulation layer;

patterning the gate conductive layer to form a gate electrode crossing the active region; and

forming a sidewall spacer on a sidewall of the gate electrode.

8. (Previously presented) The method of claim 7, in which the forming the source/drain region of second conductivity type comprises:

after forming the gate electrode,

implanting impurity ions into a first surface region of the active region to form a lightly diffused layer into the first surface region at both sides of the gate electrode; and

after forming the sidewall spacer,

implanting impurity ions into a second surface region of the active region to form a heavily diffused layer into the second surface region at both sides of the gate electrode with sidewall spacer;

the heavily diffused layer formed with a depth deeper than the depth of the lightly diffused layer.

9. (Original) The method of claim 5, in which the siliciding comprises:

forming metal on the exposed surface of the source/drain region and on the portion of the substrate of first conductivity type exposed by the recess; and

annealing the metal on the exposed surfaces to silicide a surface of the source/drain region of second conductivity type in contact with the metal and to silicide a surface of the substrate of first conductivity type in contact with the metal and facing the recess.

10. (Original) The method of claim 9, in which the siliciding further comprises siliciding a top surface of the gate electrode to form a gate salicide layer.

11. (Original) The method as claimed in claim 9, in which the metal comprises at least one of cobalt, nickel, and titanium.

12. (Previously presented) A method of fabricating a semiconductor device, comprising:

forming a device isolation layer in a semiconductor substrate having N-type and P-type regions;

the device isolation layer defining first and second active regions in the N-type and P-type regions, respectively;

forming first and second gate patterns crossing the first and second active regions, respectively;

forming a P-type source/drain region in the first active region at both sides of the first gate pattern;

forming an N-type source/drain region in the second active region at both sides of the second gate pattern;

patterning the device isolation layer to form first and second recesses;

the first recess exposing a portion of the N-type region of the substrate adjacent to the P-type source/drain region at one side of the first gate pattern;

the second recess to exposing a portion of the P-type region of the substrate adjacent to the N-type source/drain region at one side of the second gate pattern; and

siliciding the exposed portions of the N-type and P-type regions facing respective first and second recesses; and

siliciding surfaces of the N-type and P-type source/drain regions of respective second and first active regions.

13. (Previously presented) The method of claim 12, in which the forming the first and second gate patterns comprises:

sequentially forming a gate insulation layer and a gate conductive layer on the first and second active regions;

patterning the gate conductive layer to form first and second gate electrodes that cross the first and second active regions, respectively; and

forming spacers on sidewalls of each of the first and second gate electrodes.

14. (Previously presented) The method as claimed in claim 13, in which the forming the N-type and P-type source/drain regions comprises:

after forming the first and second gate electrodes:

implanting P-type impurity ions into the first active region to form a lightly diffused P-type layer; and

implanting N-type impurity ions into the second active region to form a lightly diffused N-type layer; and

after forming the first and second sidewall spacers:

implanting P-type impurity ions into the first active region to form a heavily diffused P-type layer of depth deeper than the lightly diffused P-type layer; and

implanting N-type impurity ions into the second active region to form a heavily diffused N-type layer of depth deeper than the lightly diffused N-type layer.

15. (Original) The method of claim 12, in which the first and second recesses are formed by etching the device isolation layer to a depth deeper than the P-type and N-type source/drain regions.

16. (Original) The method of claim 12, in which the siliciding comprises:

forming metal on exposed surfaces including walls of the first and second recesses; and

annealing the metal and siliciding surfaces of the P-type and N-type source/drain regions in contact with the metal and siliciding the exposed surfaces of N-type and P-type materials of the substrate in contact with the metal within the first and second recesses respectively.

17. (Original) The method of claim 16, in which the metal layer comprises at least one of cobalt, nickel and titanium.